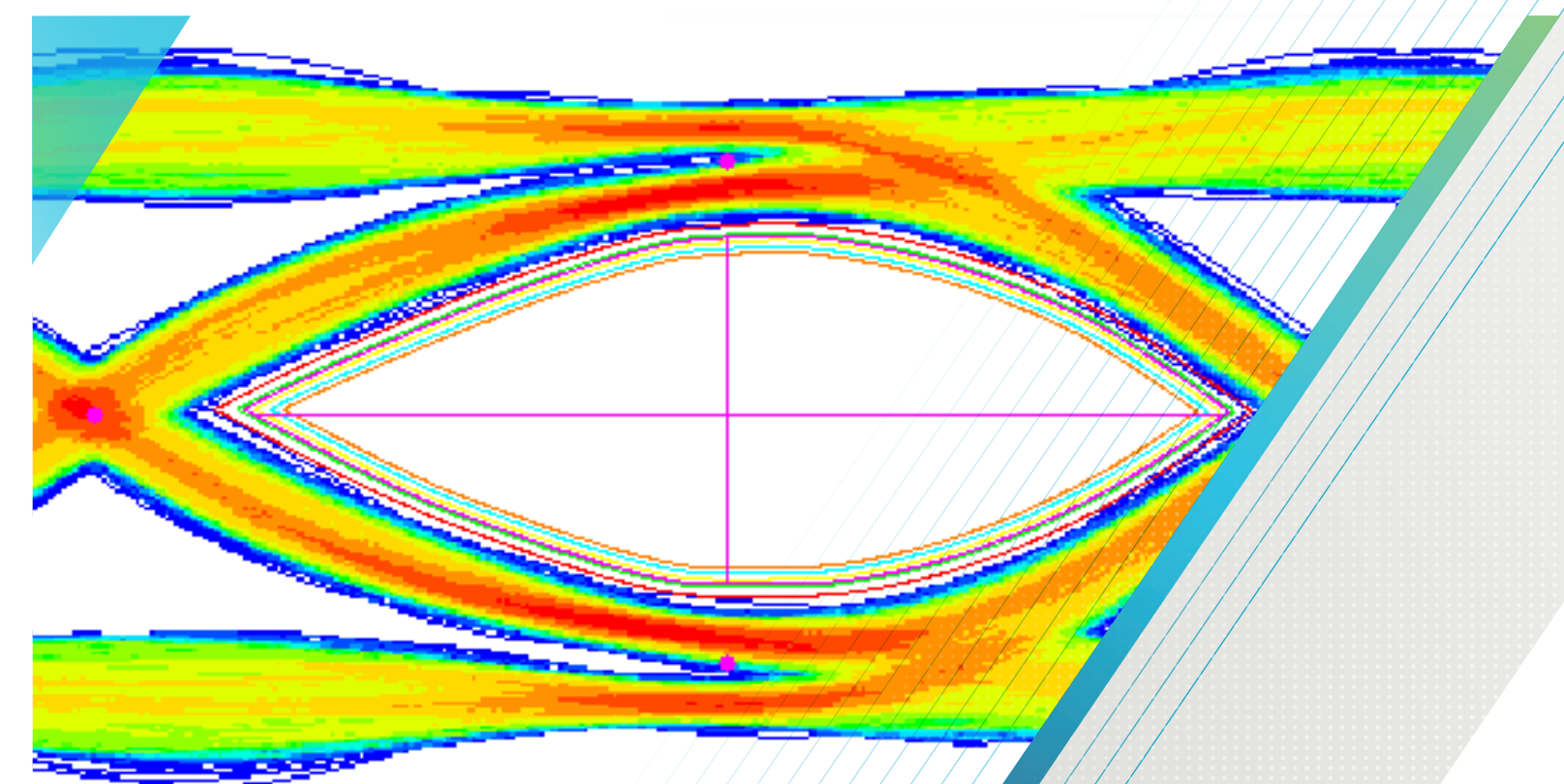


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 Vietnam 12060128

MIPI® Testing Challenges and Solutions

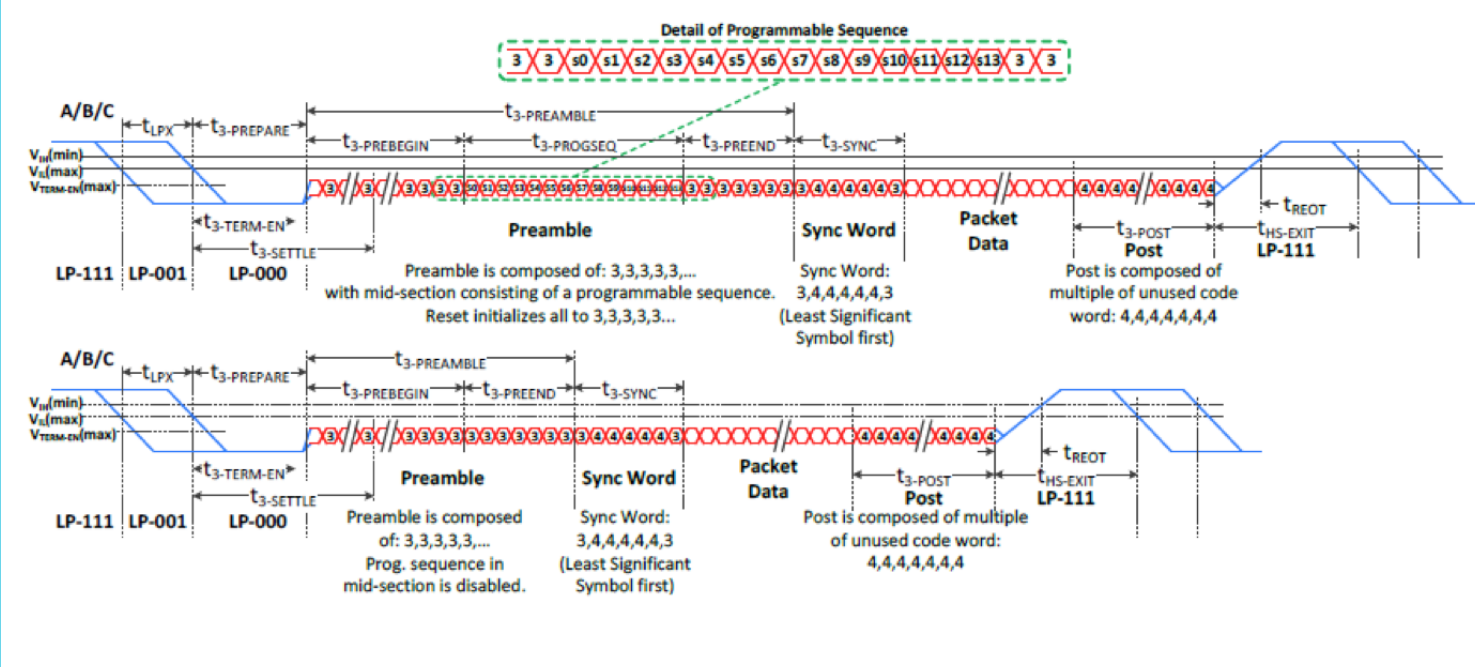
POSTER



MIPI® Testing Challenges and Solutions

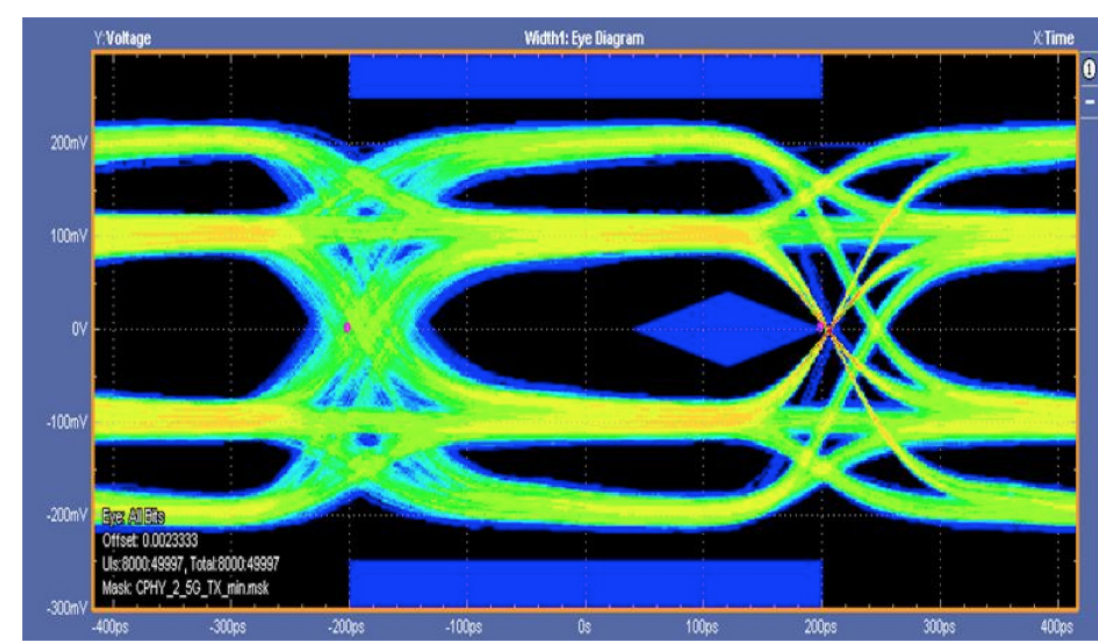
MIPI C-PHYSM for Camera & Display Interfaces

Applications	Camera & Display
Protocols	CSI-2, DSI-2
Clocking	Embedded
Channel Compensation	Encoding to reduce data toggle rate
Signaling	3-level signaling over 3 wires, Dynamic LP-HS Transition
Minimum Pins	3 (Data)
High Speed Data Rate	3.0GS/s
Encoding	16 Bit - 7 Symbol



C-PHY TX Testing

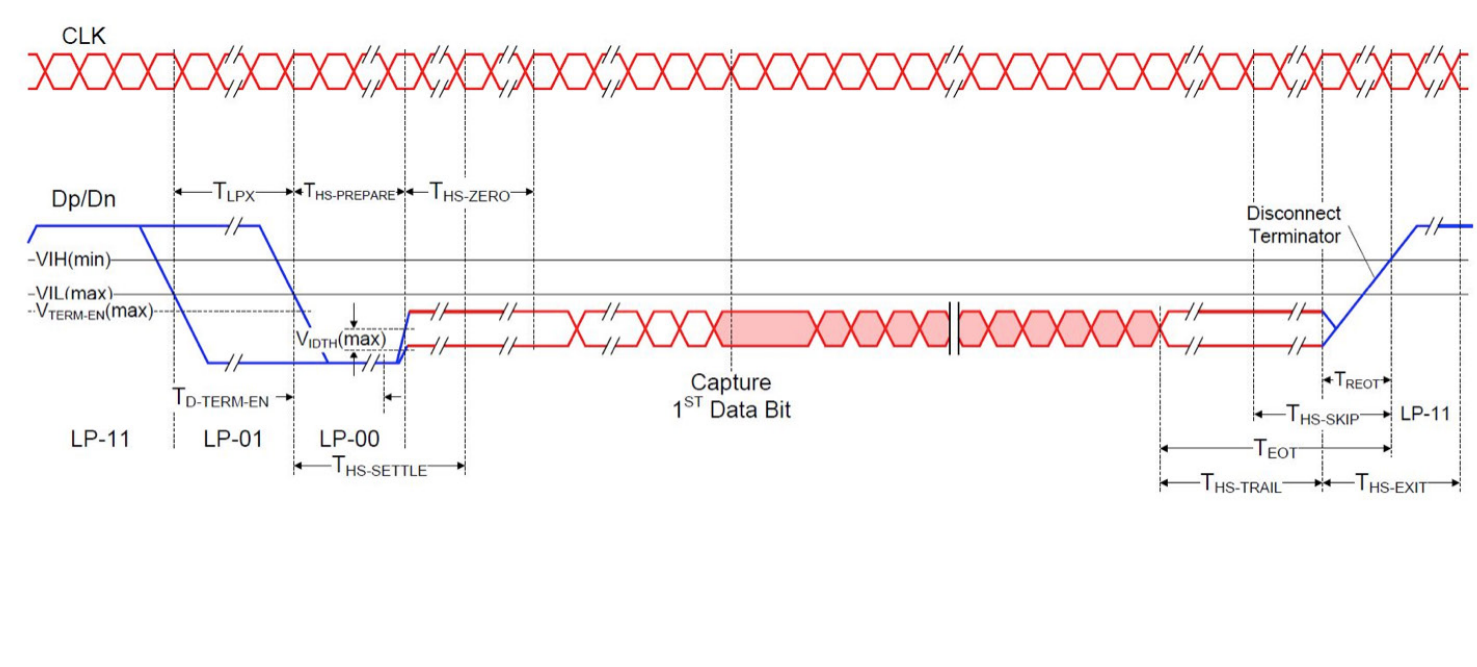
- Challenge:** Identify LP-HS transitions to constrain signal analysis
Solution: Trigger on LP Entry & Exit events
- Challenge:** Test to TX pin to verify conformance
Solution: De-embed lossy structures between the TX pin and scope
- Challenge:** Perform >100 complex combinations of TX measurements
Solution: Automation software covers full TX test suite
- Challenge:** Verify bus performance under various data rates
Solution: Analysis solution detects bus speed, and adjusts analysis and limits accordingly
- Challenge:** Verify TX signal quality using triggered eye diagram
Solution: Clock recovery algorithm which detects 1st UI edge, renders eye diagram, and auto-adjusts mask



Eye Diagram at 2.5GS/s

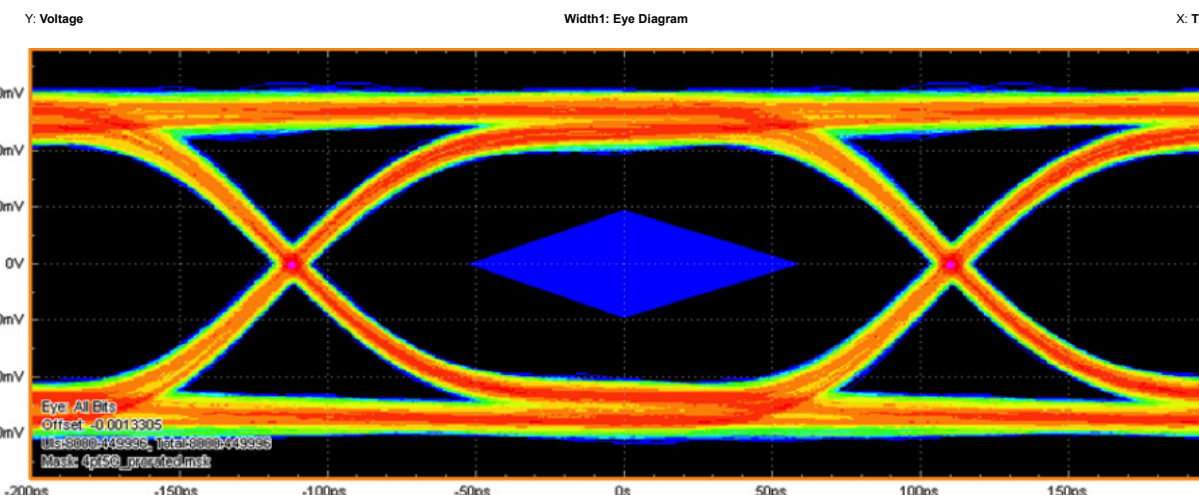
MIPI D-PHYSM for Camera & Display Interfaces

Applications	Camera & Display
Protocols	CSI-2, DSI-2
Clocking	Source Synchronous, SSC
Channel Compensation	Data skew control relative to clock
Signaling	NRZ, Dynamic LP-HS Transition
Minimum Pins	4 (2 Data + 2 Clock)
High Speed Data Rate	500Mb/s - 4.5Gb/s
Encoding	8b9b



D-PHY TX Testing

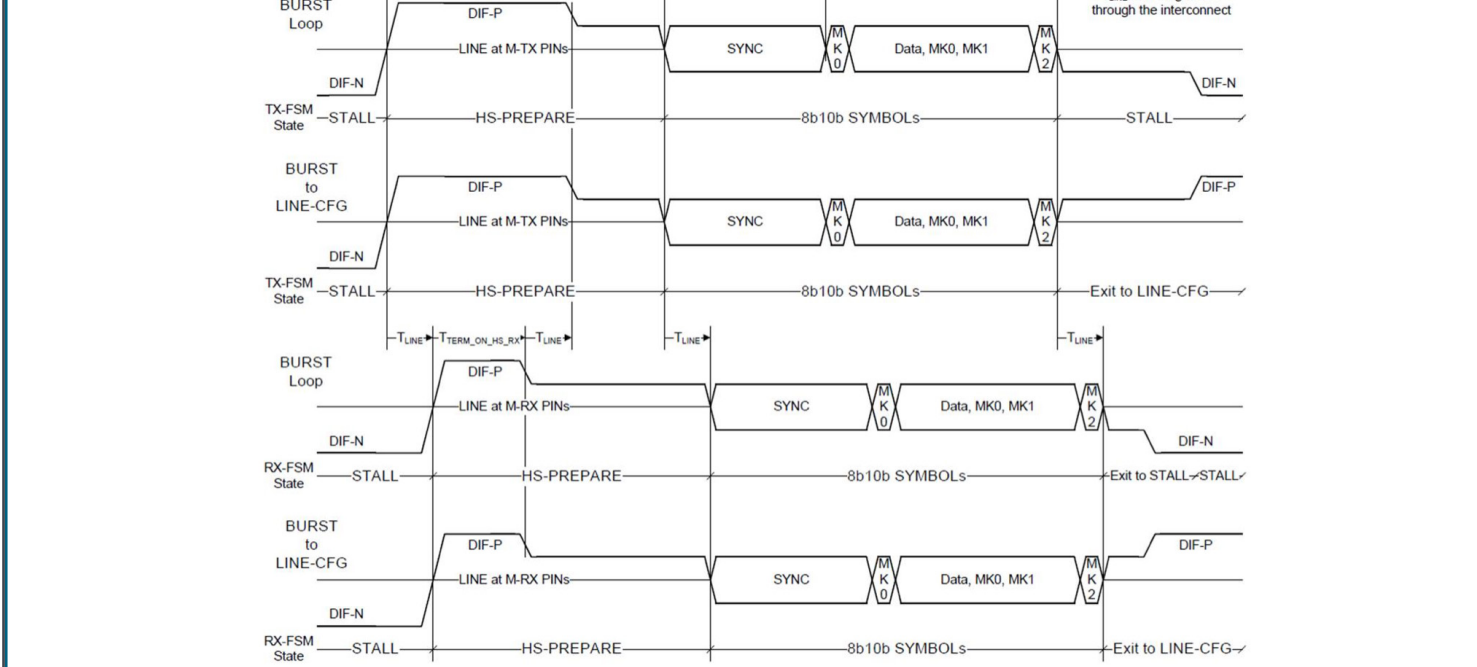
- Challenge:** Verify LP & HS TX performance with dynamically switching termination
Solution: A well designed switch-able termination board with easy probe point access
- Challenge:** Measure voltage and timing parameters for LP Mode, HS Mode, and LP-HS transitions
Solution: Mode-specific TX measurements for LP, HS, and LP-HS
- Challenge:** Test performance on multiple lanes
Solution: Insert RF switch for multi-lane testing, de-embed switch effects
- Challenge:** Ensure transmitter provides minimum signal quality performance
Solution: Perform eye diagram test with extrapolation to BER 10⁻¹²
- Challenge:** Locate and root cause packet corruption issues
Solution: Capture and decode live traffic using Oscilloscope, correlate packet errors back to signal quality issues



Eye Diagram at 4.5Gbps

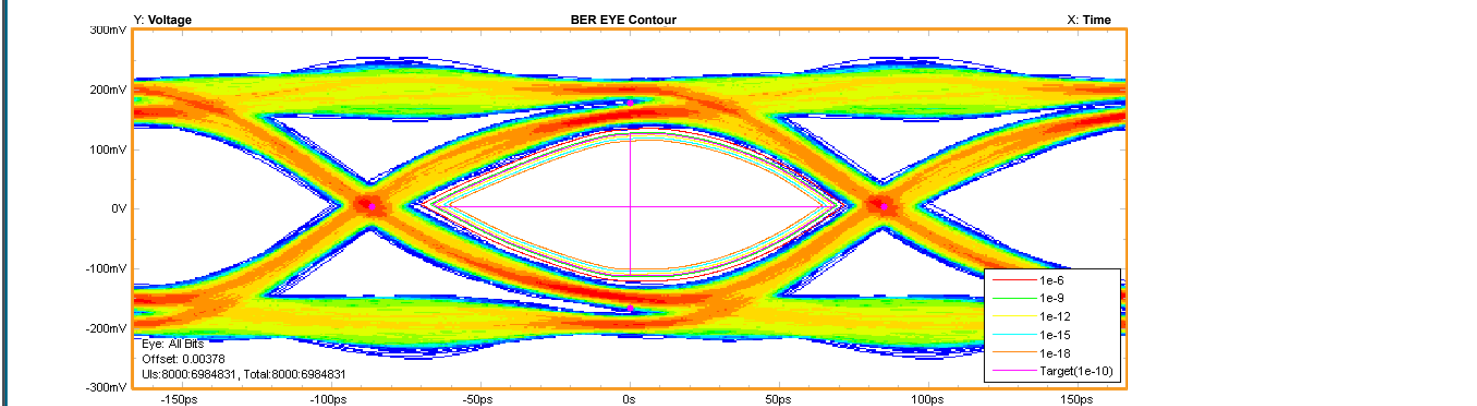
MIPI M-PHYSM for Storage Interfaces

Applications	Storage Devices, Modem Chips, GPS, RFIC, Companion Chip
Protocols	UniPro, UFS, SSIC, PCIe
Clocking	Embedded
Channel Compensation	Equalization (CTLE+DFE at HS G4)
Signaling	NRZ for High Speed, Distinct PWM Mode for Low Power
Minimum Pins	2 (Data)
High Speed Data Rate	1.5Gb/s - 11.6Gb/s
Encoding	8b10b



M-PHY TX Testing

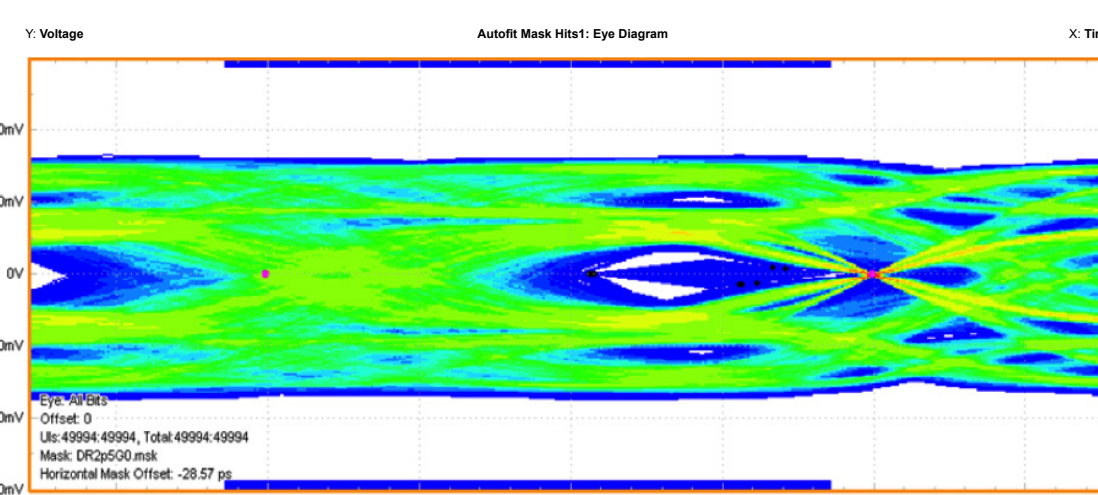
- Challenge:** Support measurements for High Speed Mode, PWM Mode and SYS Mode in Continuous and Burst operation
Solution: Algorithms that detect different modes and perform appropriate analysis
- Challenge:** Accumulate 3 Million UIs quickly to validate different eye masks for different gears
Solution: Acquire 3 Million UIs in a single acquisition, render eye diagram, auto position mask, and perform required measurements
- Challenge:** Simulate signals with Channel effect and apply equalization techniques to ensure that the Transmitter (TX) meets the needs of the Receiver (RX)
Solution: Create embed filter files to simulate the channel effect and apply equalization of CTLE+DFE per the specification
- Challenge:** Measure signals across 100 Ohms differential termination without any signal quality compromise. Meet specification return loss requirements while maintaining high common mode input impedance
Solution: Low noise, high sensitivity active probes with adjustable V-Term capability to control common mode voltage with minimal signal attenuation
- Challenge:** Eye Diagram test with extrapolation at BER 10⁻¹⁰
Solution: Sophisticated BER contour eye diagram extrapolation methods coupled with jitter analysis tools



Eye Diagram at High Speed G3B with BER Contours

C-PHY RX Testing

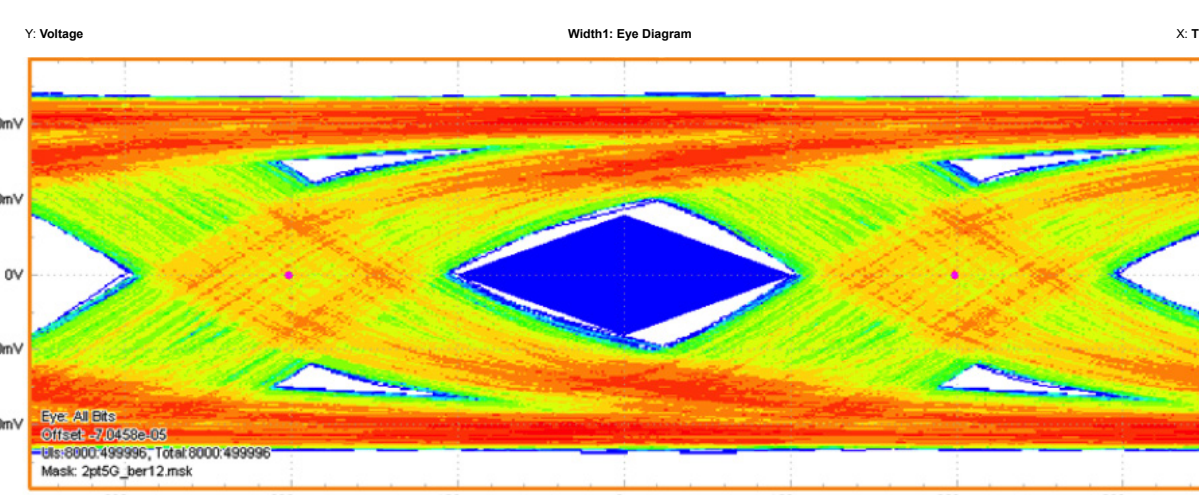
- Challenge:** Generate LP-only, HS-only, & LP-HS transitions for data rate up to 3 GS/s
Solution: Configurable pattern generators capable of multi-level signaling
- Challenge:** Generate device-specific patterns and sequences needed to initiate internal error detector mode
Solution: Flexibility in pattern creation and sequencing
- Challenge:** Provide high-margin components that work when integrated into a lossy system design
Solution: Sweep stress parameters from the pattern generator to find performance boundaries
- Challenge:** Ensure receiver can handle different combinations of voltages
Solution: Sweep combinations of common mode, high and low voltages to verify receiver performance
- Challenge:** Ensure receiver can operate at max designed speed with specified stresses applied to three single-ended data lanes
Solution: Use a pattern generator with superior DAC resolution, bandwidth response, and sample rate



Stressed Eye Diagram with DCD

D-PHY RX Testing

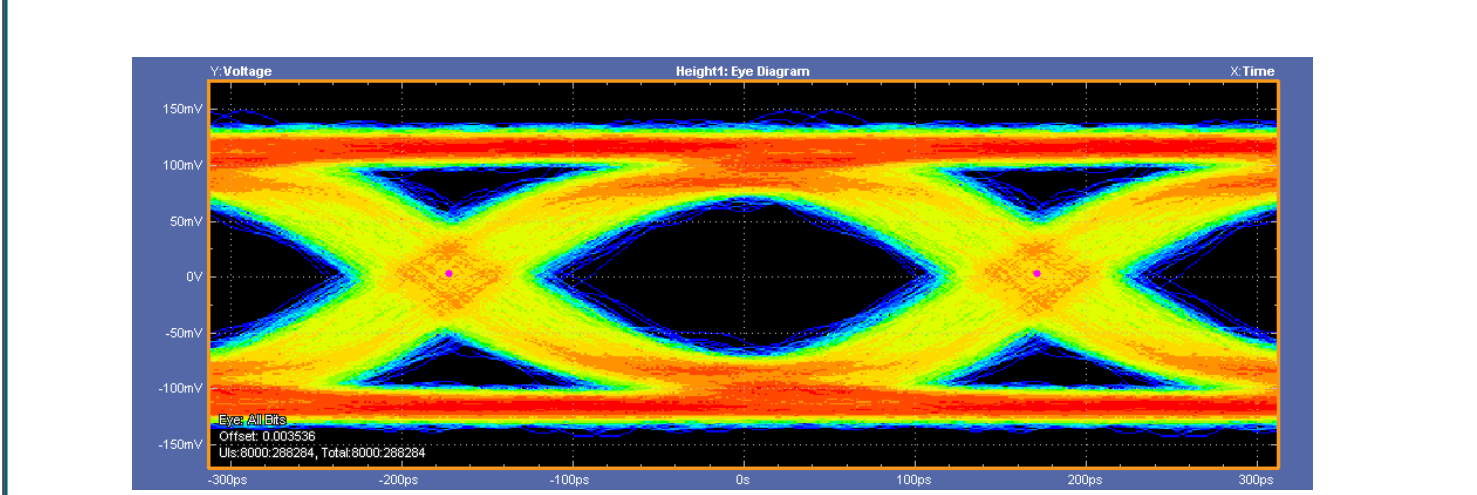
- Challenge:** Generate LP-only, HS-only, & LP-HS transitions for data rates up to 4.5Gb/s
Solution: Configurable pattern generators capable of multi-level signaling
- Challenge:** Generate test pattern with option to turn on SSC and add stress parameters like jitter, static and dynamic skew, common mode noise, ISI, etc.
Solution: Synthesis software that produces required stresses and yields statistically rich behavior
- Challenge:** Test to the RX pin to verify conformance
Solution: Embed lossy structures to calibrate stress generator
- Challenge:** Verify LP mode not susceptible to interference and crosstalk
Solution: Add eSpike, common mode noise, and jitter to LP Mode test signals
- Challenge:** Ensure receiver can handle different timing and skew parameters
Solution: Sweep bus timings including rise/fall times and clock-to-data skew to verify receiver performance



Stressed Eye Diagram with Dynamic Skew

M-PHY RX Testing

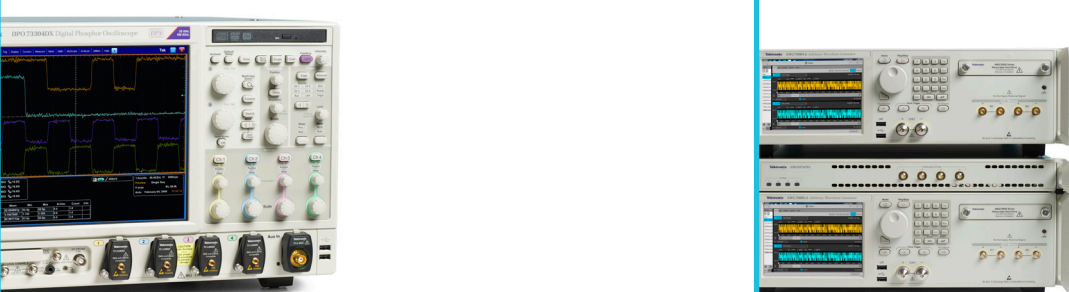
- Challenge:** Generate test pattern with stresses like jitter, static and dynamic skew, common mode noise, ISI, etc.
Solution: Synthesis software that produces required stresses and yields statistically rich behavior
- Challenge:** Generate device-specific patterns and sequences needed to initiate internal error detector mode
Solution: Flexibility in pattern creation and sequencing
- Challenge:** Test to the RX pin to verify conformance
Solution: Embed lossy structures to calibrate stress generator
- Challenge:** Provide high-margin components that work when integrated into a lossy system design
Solution: Sweep stress parameters from the pattern generator to find performance boundaries
- Challenge:** Ensure receiver can handle different combinations of voltages
Solution: Set common mode and voltage swing of test signals, and sweep these voltages to verify receiver margin



Stressed Eye with SJ Sweep

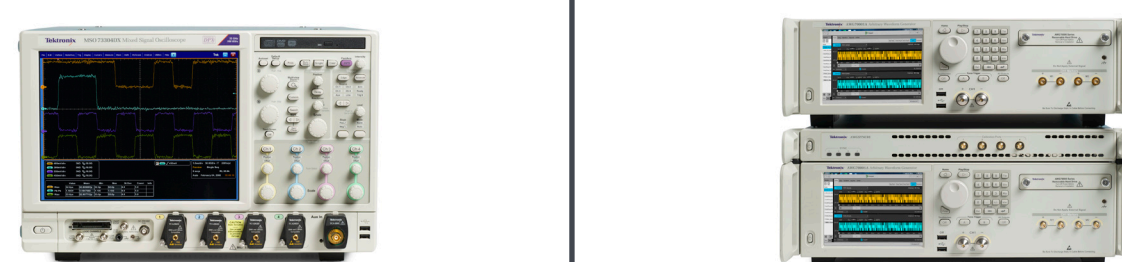
C-PHY Suggested Solutions

- TX Testing**
 - 4 Channel Real-Time Oscilloscope with a minimum of 6 GHz Bandwidth (Tektronix DPO/MSO70000C or 70000DX Series)
 - High Impedance Probe (Tektronix P7300 Series)
 - MIPI Termination Board (Tektronix TMPC-CTB)
- RX Testing**
 - 2 Arbitrary Waveform Generators with a minimum Channel Sample Rate of 12 GS/s (Tektronix AWG7000 or AWG70000 Series)
 - Synchronization Hub (Tektronix AWGSYNC01)
 - MIPI Signal Combiner
 - Low Pass HW Filters to adjust rise time (Tektronix PSPL5915)



D-PHY Suggested Solutions

- TX Testing**
 - 4 Channel Real-Time Oscilloscope with a minimum of: 1.5Gbps and 4 GHz Bandwidth 2.5Gbps and 8 GHz Bandwidth (Tektronix DPO/MSO70000C or 70000DX Series)
 - MIPI Termination Board (Tektronix TMPC-CTB)
 - High Impedance Probe (Tektronix P7300 Series)
- RX Testing**
 - 2 Arbitrary Waveform Generators with a minimum Channel Sample Rate of 12 GS/s (Tektronix AWG7000 or AWG70000 Series)
 - Synchronization Hub (Tektronix AWGSYNC01)
 - MIPI Signal Combiner
 - Low Pass HW Filters to adjust rise time (Tektronix PSPL5915)



M-PHY Suggested Solutions

- TX Testing**
 - 4 Channel Real-Time Oscilloscope with a minimum: Gear 1 - 8.5 GHz Bandwidth Gear 2 - 6 GHz Bandwidth Gear 3 - 12.5 GHz Bandwidth Gear 4 - 23 GHz Bandwidth (Tektronix DPO/MSO70000C or 70000DX Series)
 - Differential SMA Probe with Vterm (Tektronix P7600 Series or P7313SMA)
- RX Testing**
 - A BERTScope with a minimum: Gear 1 - 8.5 GHz Bandwidth Gear 2 - 8.5 GHz Bandwidth Gear 3 - 8.5 GHz Bandwidth Gear 4 - 12.5 GHz Bandwidth (Tektronix BSA85C or BSA125C BERTScope)
 - ISI Board (Variable -ACE Unitek CLE1000-A2 for G1/G2, CLE1000-S2 for G3)
 - Low Pass HW Filters to adjust rise time (Tektronix PSPL5915)
 - Arbitrary/Function Generator (Tektronix AFG3252C)

